NASA Electronic Parts and Packaging (NEPP) Program FPGA Radiation Collaboration Update for FY18

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Outline

- Task Overview
- FY18 Targeted Test Devices
- Test Approach and Designs
- Test Setup
- Test Results
- Future Plans

NEPP – Processors, Systems on a Chip (SOC), and Field Programmable Gate Arrays (FPGAs)

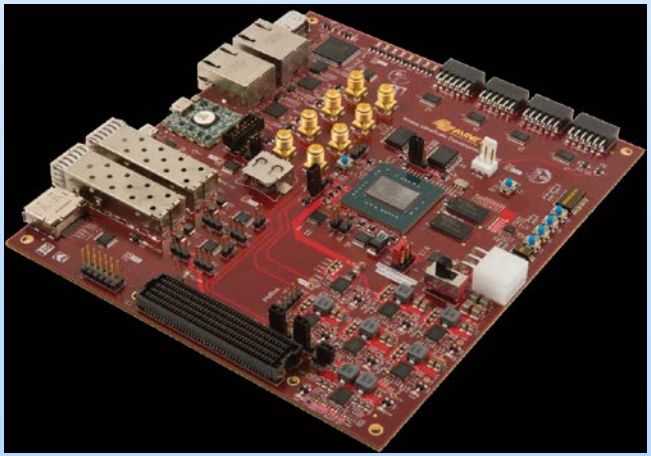
Task Objectives

- **Perform Total Ionizing Dose (TID) testing of state of the art FPGA technologies, including, but not limited to, Intel Cyclone 10 and Xilinx UltraScale, as available.**
- **Provide technical test planning, preparation, and execution assistance to parallel task at GSFC, lead by Melanie Berg.**
- **Expected deliverables include test reports for every JPL-lead test effort, and an inclusive year-end report describing all testing, results, and lessons learned. Monthly and quarterly review charts will be provided to management as required.**

Targeted Test Devices

Device	Node Technology (nm)	Logic Cells (K)	DSP Slices	Block RAM (Mb)	PLL	Transceivers	I/O Pins
XCKU040	TSMC 20	530	1,920	21.1	10	16 (12.5 Gb/s)	468
10CX220	TSMC 20	220	192	12.5	10	16 (12.5 Gb/s)	284

Qty	Part Number	Package	Evaluation Board	Availability
3	XCKU040-1FBVA676	BBGA-676	AES-KU040-DB (Avnet)	In stock
3	10CX220YF780E5G	FBGA-780	DK-DEV-10CX200-A (Intel)	~8 weeks lead time



Test Approach

- Modify the evaluation board to be bare bones
- Develop designs as high-speed as practical
- Ensure use of the HR IO banks

Characterization Tests

- **DC Characterization**
  - **Monitor and record all supply rails for voltage and current**
    - **High resolution current leakage monitoring**
    - **All non-essential and unrelated electrical components and devices were removed from the evaluation board with the exception of the DDR4 memories, clock oscillator, and the LVDS clock synthesizer (used for GTH)**

Characterization Tests

- **AC Characterization**
  - **Measured switching characteristics using our high speed and precise oscilloscope for various I/O standards, ring oscillators, clock buffers, Mixed-Mode Clock Manager (MMCMs/PLLs), LUTs, flip-flops, and transceivers**
    - **Rise/Fall times, propagation delay, clock skew/jitter, pulse width, slew rate, duty cycle eye-diagram profiles for differential signals (eye height/width)**
    - **Propagation delays were measured through two methods**
      - **Compare input signal and output delay on I/O pins going through internal FFs chains (shift registers) and lookup tables (LUTs, inverters)**
    - **Instantiated maximum number of MMCM/PLLs, daisy chained, and measure clock frequency, jitter, and slew rate on the oscilloscope while monitoring consistency of the phase lock**

Characterization Tests

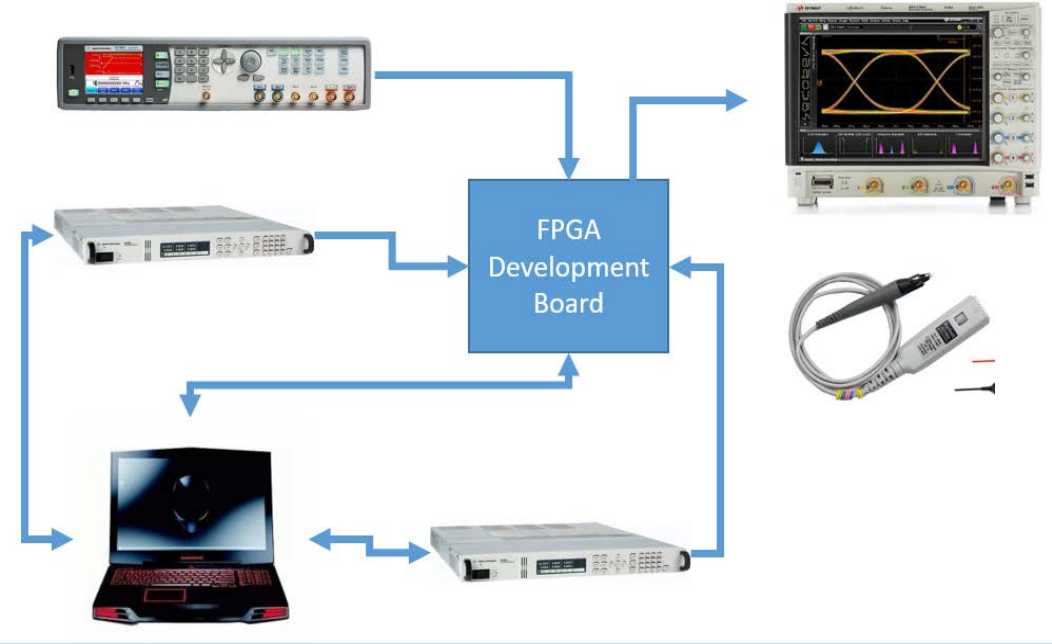
- **AC Characterization**
  - **Transceivers**
    - **Exercised the high speed GTH/GTY transceivers by outputting through the SMA connectors present on the evaluation board and also through a FMC breakout board**
      - **Used multiple transceiver banks and input clocks for variability**
      - **Loopback daisy chained**
  - **Eye-diagrams on the scope**

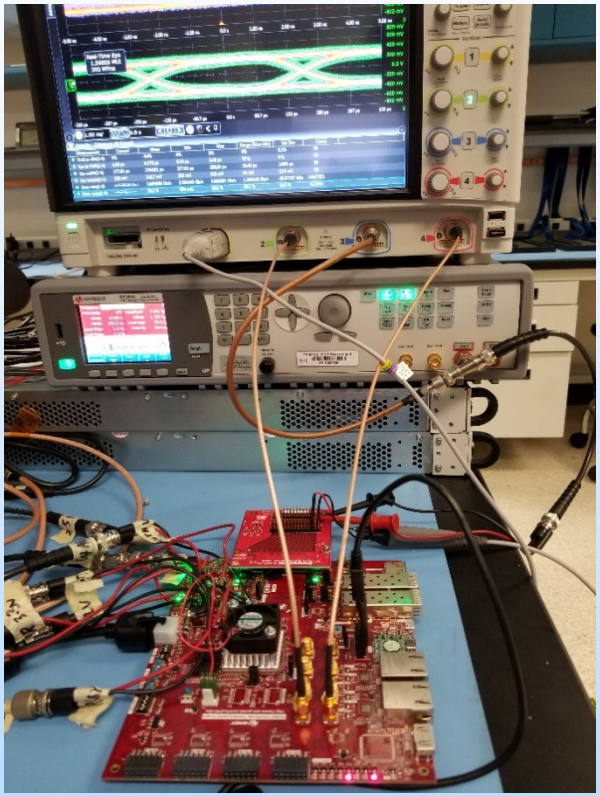
Characterization Tests

- **Functional Characterization**
  - **Example embedded design at full speed using MicroBlaze, DDR4 controller and BRAM**
  - **System Monitor (SYSMON)**
    - **Monitor and verify SYSMON interface and functionality**
      - **Can read back device temperature and device rail voltages using both software through JTAG or the SYSMON header provided on the evaluation board**
  - **BRAM**
    - **Write and read patterns to BRAM/FIFO**
  - **FPGA Configuration**
    - **CRAM functionality test for successful programming**

Preliminary (Pathfinder) Test Setup

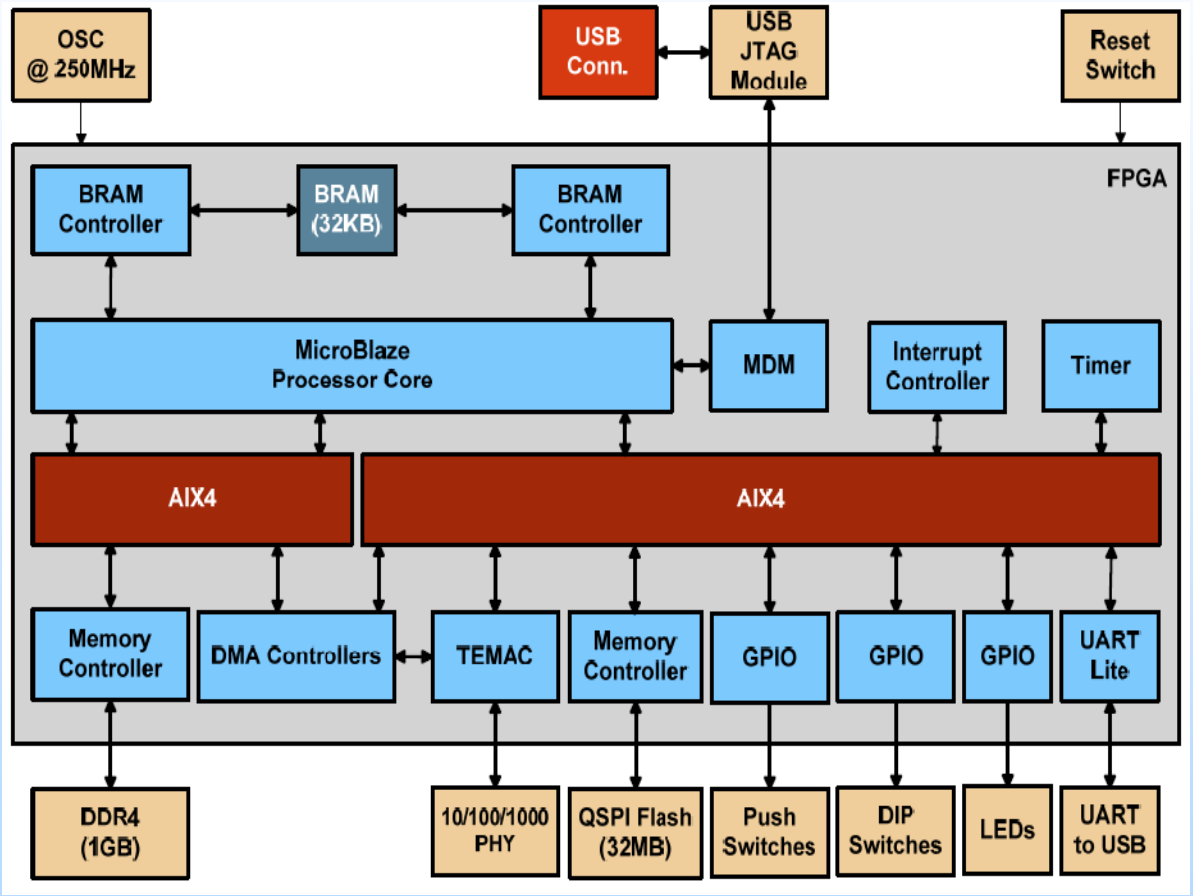
- Power Supplies
  - Two Keysight N6700B with 4 power modules each (used 7 channels)
    - Used for bench-top testing
  - Two Keysight N6705C with 4 power modules each (used 7 channels)
    - Used for biasing the device in the cell
- Pulse Generator
  - Keysight 81160A
- Oscilloscope & Probes
  - Keysight MSOS604A
  - Keysight N2795A active probes
  - Keysight N2750A active differential probes





FPGA Designs

- **TID Bias Design:**



Preliminary (Pathfinder) Test Results

- We measured both static and dynamic device currents.
- There was no significant current increase across all power rails save…
- I_{CCINT} and HR I_{CCO} at the 620 krad(Si) level, where the values increased by about 50 mA and 150 mA respectively.

DC Parametric	Pre-irradiation	160 krad(Si)	320 krad(Si)	620 krad(Si)
V_{CCINT} [V]	0.95	0.95	0.95	0.95
I_{CCINT} (FPGA not configured) [mA]	340	380	332	370
I_{CCINT} (FPGA configured) [mA]	683	705	689	742
V_{CCAUX} & V_{CCO} (HP, Bank 0/46/66) [V]	1.8	1.8	1.8	1.8
I_{CCAUX} (FPGA not configured) [mA]	200	295	224	221
I_{CCAUX} (FPGA configured) [mA]	410	402	432	453
V_{CCO} (HR, Bank 64/65, V_{ADJ} = 3.3V) [V]	3.3	3.3	3.3	3.3
I_{CCO} (FPGA not configured) [mA]	316	250	248	372
I_{CCO} (FPGA configured) [mA]	191	225	252	375
V_{CCO} (HP, Bank 44/45) [V]	1.2	1.2	1.2	1.2
I_{CCO} (FPGA not configured) [mA]	28	28	28	28.7
I_{CCO} (FPGA configured) [mA]	230	230	230	233
V_{GTAVCC} [V]	1	1	1	1
I_{GTAICC} (FPGA not configured) [mA]	50	52	46.5	46.7
I_{GTAICC} (FPGA configured) [mA]	50	52	49	48.5
$V_{GTVCCAUX}$ [V]	1.8	1.8	1.8	1.8
$I_{GTICCAUX}$ (FPGA not configured) [mA]	0	0	0	0
$I_{GTICCAUX}$ (FPGA configured) [mA]	0	0	0	0
V_{GTAVTT} [V]	1.2	1.2	1.2	1.2
I_{GTAITT} (FPGA not configured) [mA]	11.6	10.8	10.6	10.6
I_{CCAITT} (FPGA configured) [mA]	19.3	18.8	18.8	18.7

Preliminary (Pathfinder) Test Results

- Propagation delay:
  - Several different shift registers (flip-flop chains) clocked at 800 MHz
  - Even number of daisy-chained inverters.
  - A pulse generator with a frequency 10 kHz and pulse width of 200 ns was used for both tests.
- We did not observe any significant increase in the average propagation delay of the inverter chains.

Flip Flop Chain	Pre-irradiation	160 krad(Si)	320 krad(Si)	620 krad(Si)
1				
Number of FFs	32	32	32	32
Rising Propagation Delay (ns)	52.67	51.8	51.9	52.05
Falling Propagation Delay (ns)	50.96	50.6	50.7	50.8
Average Propagation Delay (ns)	51.815	51.2	51.3	51.425
Rise Time (ns)	1.1	1.05	1.02	1.02
Fall Time (ns)	1.33	1.32	1.33	1.36
Single FF Delay (ns)	1.61921875	1.6	1.603125	1.60703125
2				
Number of FFs	1024	1024	1024	1024
Rising Propagation Delay (ns)	1293	1292	1292	1929
Falling Propagation Delay (ns)	1291	1291	1291	1291
Average Propagation Delay (ns)	1292	1291.5	1291.5	1610
Rise Time (ns)	1.03	1	0.992	0.98
Fall Time (ns)	1.21	1.2	1.23	1.24
Single FF Delay (ns)	1.26171875	1.261230469	1.261230469	1.572265625
3				
Number of FFs	8192	8192	8192	8192
Rising Propagation Delay (ns)	10252	10251	10251	10251
Falling Propagation Delay (ns)	10250	10250	10250	10250
Average Propagation Delay (ns)	10251	10250.5	10250.5	10250.5
Rise Time (ns)	1.03	0.985	0.998	0.992
Fall Time (ns)	1.32	1.23	1.32	1.33
Single FF Delay (ns)	1.251342773	1.251281738	1.251281738	1.251281738
4 (internal, shift register)				
Number of FFs	1024	1024	1024	1024
Frequency (MHz)	400	400	400	400
Rise Time (ns)	0.996	0.802	0.722	0.849
Fall Time (ns)	0.872	0.825	0.831	0.873
Slew Rate (V/ns)	1.86	2.31	1.68	1.62
5 (internal, shift register)				
Number of FFs	8192	8192	8192	8192
Frequency (MHz)	400	400	400	400
Rise Time (ns)	1.001	0.81	0.722	0.861
Fall Time (ns)	0.838	0.818	0.801	0.883
Slew Rate (V/ns)	1.93	2.29	1.77	1.7

Preliminary (Pathfinder) Test Results

- Parametric measurements for the MMCM design, which consists of a single 600 MHz output (MMCM 1), dual 300 & 450 MHz outputs (MMCM 2), and an internally daisy chained design that contains 5 MMCMs linked together with a single 350 MHz output.
- All measurements were captured using the oscilloscope and high frequency active probes. There were no significant variation in frequency, pulse width, rise/fall times, and total jitter due to TID.
- Six ring oscillators with different odd-number of inverters were implemented and measured. Again, there were no significant changes in frequency, pulse width, rise/fall times, jitter, and gate delay.

MMCM	Pre-irradiation	160 krad(Si)	320 krad(Si)	620 krad(Si)
1				
Frequency (MHz)	N/A	600	600	600
Slew Rate (V/ns)	N/A	2.54	2.85	2.78
Duty Cycle (%)	N/A	45.4	45.3	46.8
-width (ns)	N/A	0.911	0.912	0.887
+ width (ns)	N/A	0.756	0.755	800
Fall Time (ns)	N/A	1.56	1.16	0.969
Rise Time (ns)	N/A	1.54	1.08	0.943
Total Jitter (ps)	N/A	423	398	370
2				
Frequency (MHz)	300	300	300	300
Slew Rate (V/ns)	2.66	3.53	4.07	3.49
Duty Cycle (%)	48.1	48.7	49.1	49.8
-width (ns)	1.73	1.71	1.7	1.67
+ width (ns)	1.6	1.62	1.64	1.66
Fall Time (ns)	1.04	1.13	1.12	1.12
Rise Time (ns)	1.1	1.18	1.12	1.13
Total Jitter (ps)	301.5	277	251	243
2				
Frequency (MHz)	446	450	450	450
Slew Rate (V/ns)	1.63	2.53	1.66	2.54
Duty Cycle (%)	43.3	42	42.9	47.2
-width (ns)	1.29	1.29	1.27	1.17
+ width (ns)	0.974	0.932	0.951	1.05
Fall Time (ns)	0.81	1.72	0.99	1.19
Rise Time (ns)	0.921	1.52	1.1	1.19
Total Jitter (ps)	814	507	621	356
3 (Daisy Chain)				
Frequency (MHz)	350	350	350	350
Slew Rate (V/ns)	3.38	3.93	4.53	3.2
Duty Cycle (%)	40.1	43.5	47.5	45.4
-width (ns)	1.71	1.61	1.5	1.56
+ width (ns)	1.46	1.24	1.35	1.3
Fall Time (ns)	1.12	1.08	0.967	1.11
Rise Time (ns)	0.977	0.961	0.726	0.855
Total Jitter (ps)	690	581	446	544

MMCM/PLL and Ring Oscillator

Preliminary (Pathfinder) Test Results

- We tested our transceivers at 3, 1.5, and 2.5 Gbps respectively. GTH 1 is a single GTH quad using the LVDS_Clk1_C clock, GTH 2 is a single GTH quad using the LVDS_Clk0_C clock, and GTH 3 is a single GTH quad with three instantiated ports that are externally daisy chained with SMA cables.
- All three GTH quads use different clocks and banks; this was done on purpose for variability.
- For all measurements, SMA connectors from the evaluation board and a FMC to LVDS-SMA breakout board were used. SMA cables were 50Ω terminated on the scope as differential signals between channels 1-3 and 2-4.
- There were no significant changes due to TID.

GTH (SMA LVDS)	Pre-irradiation	160 krad(Si)	320 krad(Si)	620 krad(Si)
1				
Frequency /Rate (Gbps, raw data)	3	3	3	3
Eye Height (mV)	299	293	303	310
Eye Width (ps)	275	275	278	276
Duty Cycle (%)	51.1	50.7	49.1	50.2
Duty Cycle Dist (ps)	18	18.1	17.3	17
Eye Jitter RMS (ps)	6.4	6.41	6.94	6.4
2				
Frequency /Rate (Gbps, raw data)	1.5	1.5	1.5	1.5
Eye Height (mV)	346.7	293.3	265	296
Eye Width (ps)	617.6	607.4	606	608
Duty Cycle (%)	50	50	49.6	50
Duty Cycle Dist (ps)	17.17	18.3	17.9	17.3
Eye Jitter RMS (ps)	5.88	6.209	7.17	6.28
3 (Daisy Chain Externally)				
Frequency /Rate (Gbps, raw data)	2.5	2.5	2.5	2.5
Eye Height (mV)	478	466	458	460
Eye Width (ps)	346	344	348	347
Duty Cycle (%)	49.8	50.3	50.4	50
Duty Cycle Dist (ps)	11.17	13.4	12.35	10.5
Eye Jitter RMS (ps)	5.79	5.84	5.85	5.87

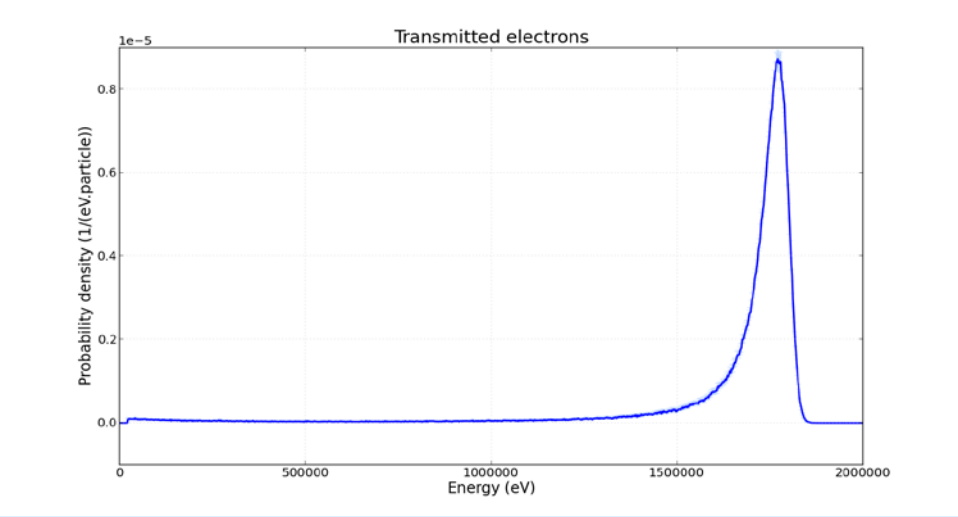
GTH (SMA LVDS)	Pre-irradiation	160 krad(Si)	320 krad(Si)	620 krad(Si)
V_{GTAVCC} [V]	1	1	1	1
I_{GTAICC} (FPGA configured) [mA]	427	424	429	431
$V_{GTVCCAUX}$ [V]	1.8	1.8	1.8	1.8
$I_{GTICCAUX}$ (FPGA configured) [mA]	0	0	0	0
V_{GTAVTT} [V]	1.2	1.2	1.2	1.2
I_{CCAITT} (FPGA configured) [mA]	389	389	390	392

Transceiver Eye Diagrams

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
DutCyc dist(2-4)	4%	4.5%	4%	5%	0%	0.1%	23
Eye jit RMS(2-4)	6.37 ps	6.368 ps	6.30 ps	6.42 ps	120 fs	25 fs	23
Eye width(2-4)	283.34 ps	285.124 ps	283.34 ps	292.71 ps	9.38 ps	3.105 ps	23
Eye height(2-4)	319 mV	335.3 mV	319 mV	405 mV	86 mV	28.6 mV	23
Data rate(2-4)	----------	3.004051 Gb/s	2.516217 Gb/s	3.829871 Gb/s	1.313653 Gb/s	44.93970 Mb/	6078394
Duty cycle(2-4)	----------	50.6 %	860 m%	99.6 %	98.8 %	24.2 %	345776

Future Test Plans

- Moving our test to the JPL Dynamitron to provide TID
- 2 MeV electron source
- Allows faster dose rate and targeted irradiation for ease of evaluation board testing
- Will compare results with Co60 tests
- Repeat with Intel Cyclone 10



Backup Slides

Backup

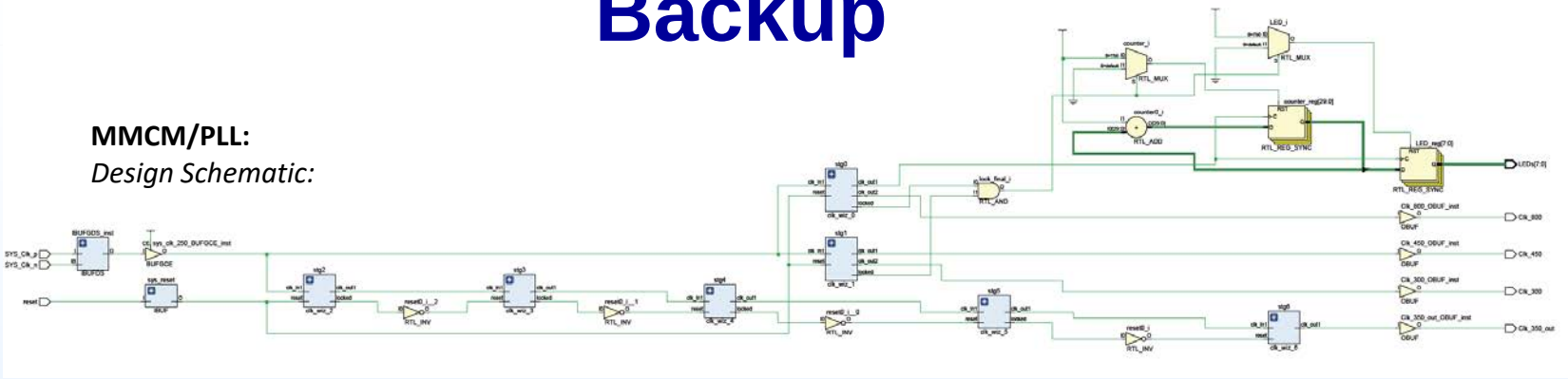
Ring Oscillator	Pre-irradiation	160 krad(Si)	320 krad(Si)	620 krad(Si)
1 (5 inverters)				
Frequency (MHz)	440	446	445	443
Slew Rate (V/ns)	2.18	2.73	2.26	2.05
Duty Cycle (%)	48	46.1	48	48.8
-width (ns)	1.23	1.21	1.17	1.16
+ width (ns)	1.19	1.04	1.08	1.1
Fall Time (ns)	0.824	0.937	0.967	1.29
Rise Time (ns)	0.689	1.1	1.11	1.49
Single Gate/LUT Delay (ps)	2.27E-10	2.24E-10	2.25E-10	2.26E-10
Clock TIE Jitter (Std Dev) [ps]	618	468	462	462
2 (25 inverters)				
Frequency (MHz)	75.9	76.1	75.8	75.7
Slew Rate (V/ns)	1.66	1.14	1.06	1.08
Duty Cycle (%)	49.3	49.6	49.3	49.4
-width (ns)	6.5	6.63	6.68	6.68
+ width (ns)	6.67	6.52	6.5	6.53
Fall Time (ns)	N/A	N/A	N/A	N/A
Rise Time (ns)	N/A	N/A	N/A	N/A
Single Gate/LUT Delay (ps)	2.63505E-10	2.62812E-10	2.63852E-10	2.64201E-10
Clock TIE Jitter (Std Dev) [ps]	165	75.1	48.6	66.7
3 (99 inverters)				
Frequency (MHz)	17.9	17.9	17.9	17.8
Slew Rate (V/ns)	2.89	3.15	3.08	3.22
Duty Cycle (%)	50	50.1	50.1	50.1
-width (ns)	27.6	27.9	28	28
+ width (ns)	28	27.9	28.1	28.1
Fall Time (ns)	1.03	0.991	1.02	0.975
Rise Time (ns)	0.949	0.862	0.853	0.812
Single Gate/LUT Delay (ps)	2.82151E-10	2.82151E-10	2.82151E-10	2.83736E-10
Clock TIE Jitter (Std Dev) [ps]	19	46.3	33.4	37.5

Ring Oscillator	Pre-irradiation	160 krad(Si)	320 krad(Si)	620 krad(Si)
4 (501 inverters)				
Frequency (MHz)	3.55	3.46	3.45	3.44
Slew Rate (V/ns)	2.63	2.75	2.58	2.9
Duty Cycle (%)	50	50.1	50.1	50.1
-width (ns)	140.7	144	145	145
+ width (ns)	141.2	145	145	145
Fall Time (ns)	1.26	1.22	1.28	1.24
Rise Time (ns)	1.01	0.965	1.02	0.935
Single Gate/LUT Delay (ps)	2.81128E-10	2.8844E-10	2.89277E-10	2.90117E-10
Clock TIE Jitter (Std Dev) [ps]	123	109	130	135
5 (2501 inverters)				
Frequency (MHz)	0.694	0.698	0.695	0.694
Slew Rate (V/ns)	2.79	2.86	2.82	2.92
Duty Cycle (%)	50	50	50	50
-width (ns)	720	717	719	721
+ width (ns)	721	717	720	721
Fall Time (ns)	1.22	1.19	1.23	1.23
Rise Time (ns)	0.952	0.928	0.94	0.915
Single Gate/LUT Delay (ps)	2.88069E-10	2.86418E-10	2.87655E-10	2.88069E-10
Clock TIE Jitter (Std Dev) [ps]	159	167	237	187
6 (5001 inverters)				
Frequency (MHz)	0.346	0.346	0.345	0.345
Slew Rate (V/ns)	2.78	2.83	2.79	2.91
Duty Cycle (%)	50	50	50	50
-width (ns)	1442	1442	1446	1.45
+ width (ns)	1445	1447	1449	1.45
Fall Time (ns)	1.2	1.14	1.18	0.18
Rise Time (ns)	0.945	0.915	0.939	0.911
Single Gate/LUT Delay (ps)	2.8896E-10	2.8896E-10	2.89797E-10	2.89797E-10
Clock TIE Jitter (Std Dev) [ps]	603	643	673	685

Backup

MMCM/PLL:

Design Schematic:



Utilization:

Resource	Utilization	Available	Utilization %
LUT	2	242400	0.01
FF	38	484800	0.01
IO	15	312	4.81
BUFG	17	480	3.54
MMCM	7	10	70.00

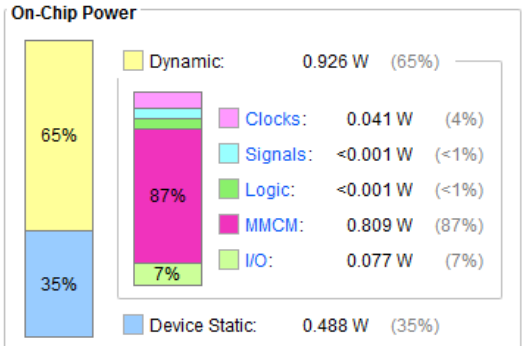
Timing:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.694 ns	Worst Hold Slack (WHS):	0.060 ns	Worst Pulse Width Slack (WPWS):	0.080 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	38	Total Number of Endpoints:	38	Total Number of Endpoints:	85

Power:

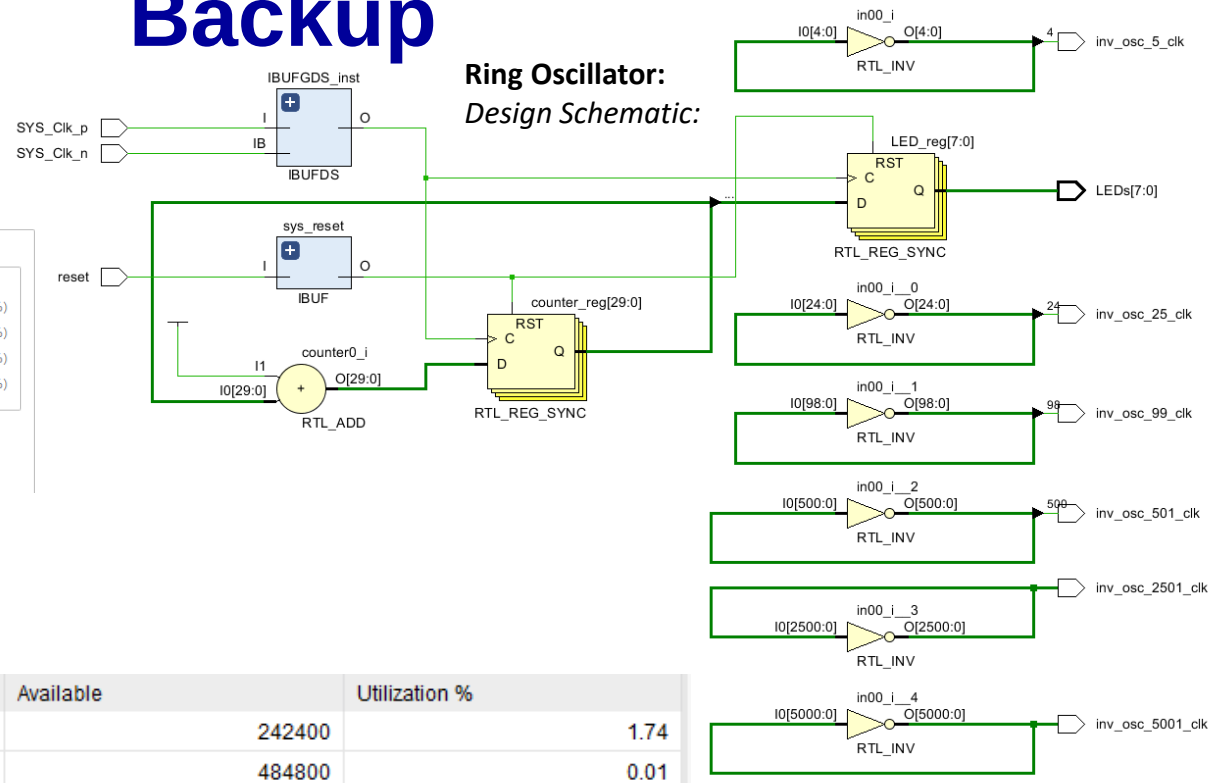
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.415 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.6°C**
Thermal Margin:	57.4°C (30.2 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium



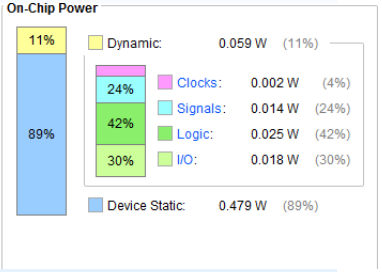
Backup

Ring Oscillator:
Design Schematic:



Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.538 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.0°C**
Thermal Margin:	59.0°C (31.0 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium



Utilization:

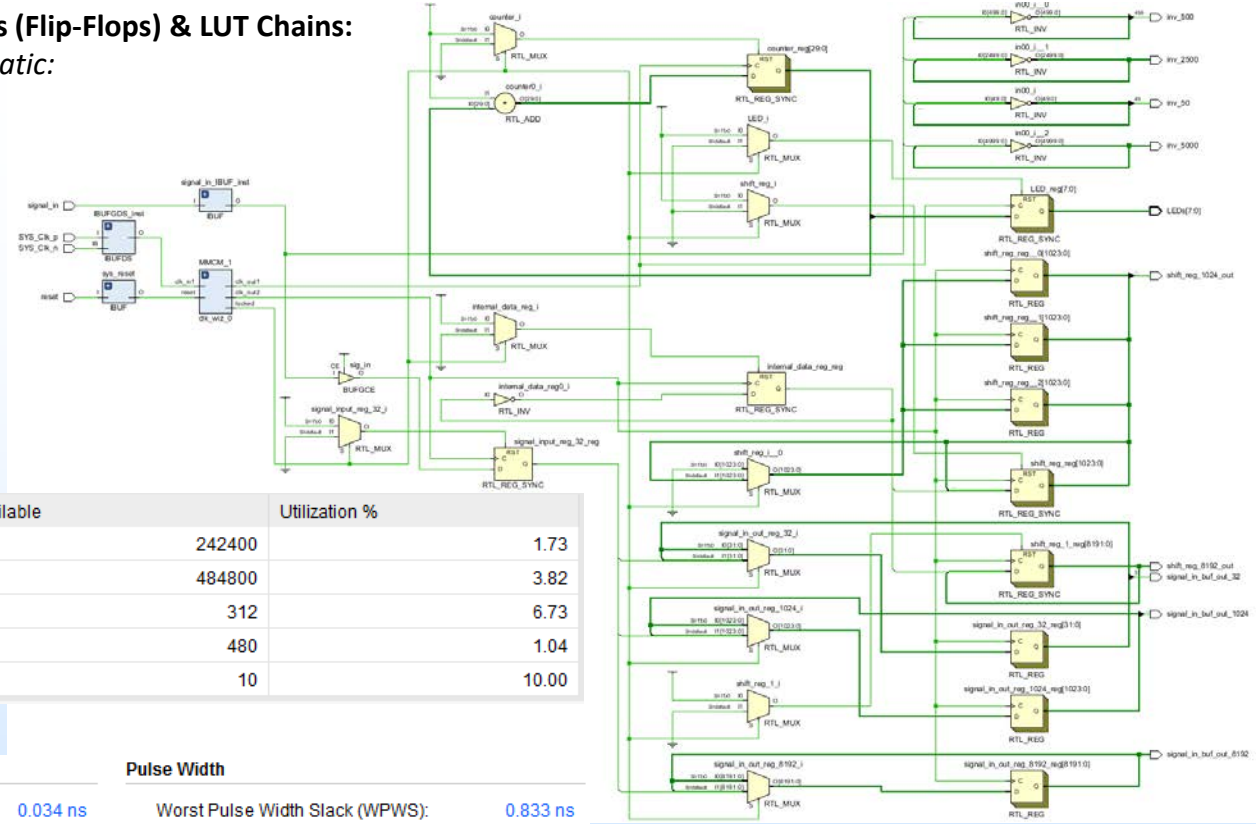
Resource	Utilization	Available	Utilization %
LUT	4212	242400	1.74
FF	38	484800	0.01
IO	17	312	5.45
BUFG	1	480	0.21

Timing:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.355 ns	Worst Hold Slack (WHS):	0.054 ns	Worst Pulse Width Slack (WPWS):	1.725 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	38	Total Number of Endpoints:	38	Total Number of Endpoints:	39

Shift Registers (Flip-Flops) & LUT Chains:

Design Schematic:



Utilization:

Resource	Utilization	Available	Utilization %
LUT	4205	242400	1.73
FF	18504	484800	3.82
IO	21	312	6.73
BUFG	5	480	1.04
MMCM	1	10	10.00

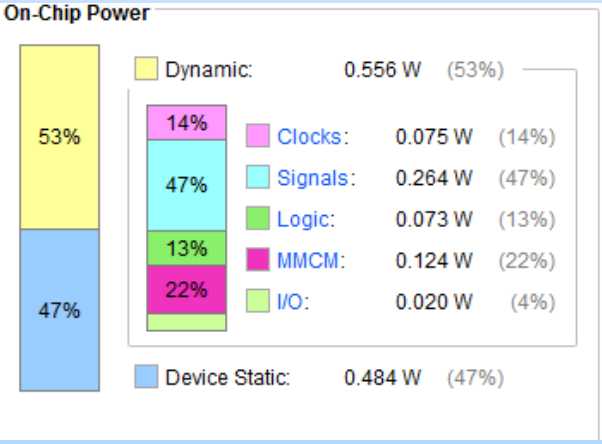
Timing:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.829 ns	Worst Hold Slack (WHS):	0.034 ns	Worst Pulse Width Slack (WPWS):	0.833 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	9255	Total Number of Endpoints:	9255	Total Number of Endpoints:	9264

Power:

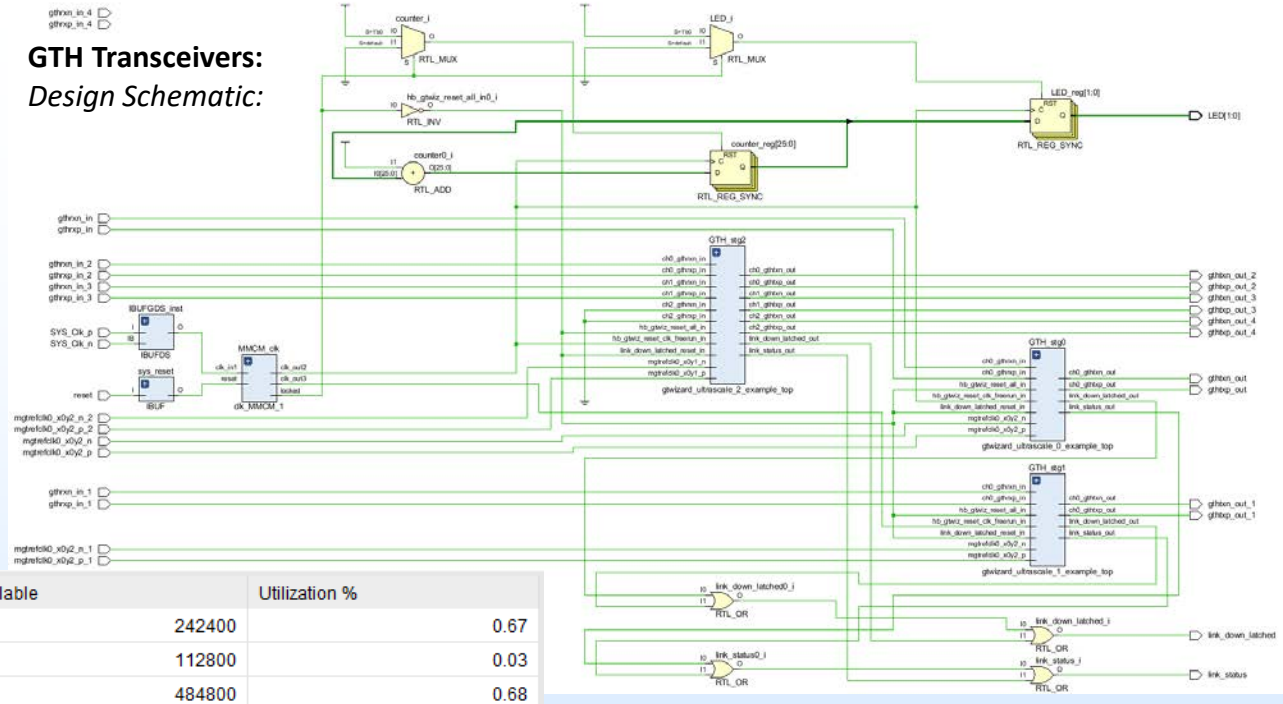
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.041 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.9°C**
Thermal Margin:	58.1°C (30.5 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium



GTH Transceivers:

Design Schematic:



Utilization:

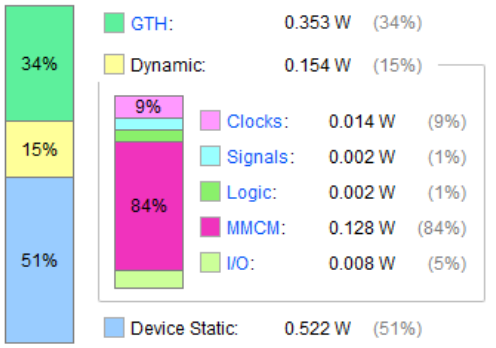
Resource	Utilization	Available	Utilization %
LUT	1635	242400	0.67
LUTRAM	32	112800	0.03
FF	3296	484800	0.68
IO	7	312	2.24
GT	5	16	31.25
BUFG	10	480	2.08
MMCM	1	10	10.00

Power:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.028 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.9°C**
Thermal Margin:	58.1°C (30.5 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

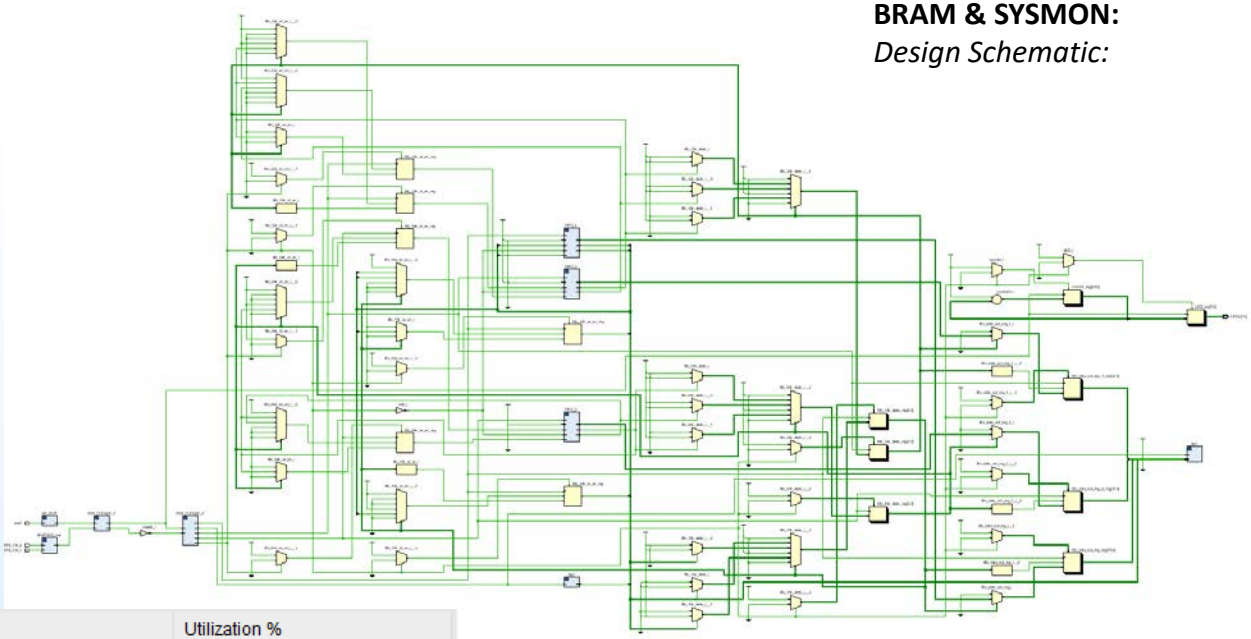
On-Chip Power



Timing:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.320 ns	Worst Hold Slack (WHS):	0.020 ns	Worst Pulse Width Slack (WPWS):	0.495 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	3774	Total Number of Endpoints:	3774	Total Number of Endpoints:	2210

BRAM & SYSMON:
Design Schematic:



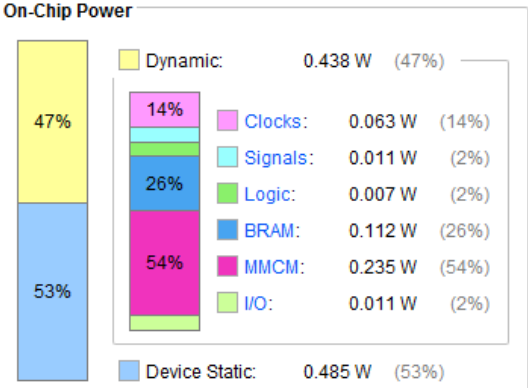
Utilization:

Resource	Utilization	Available	Utilization %
LUT	2931	242400	1.21
LUTRAM	525	112800	0.47
FF	4513	484800	0.93
BRAM	131	600	21.83
IO	11	312	3.53
BUFG	9	480	1.88
MMCM	2	10	20.00

Power:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.923 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.7°C**
Thermal Margin:	58.3°C (30.6 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

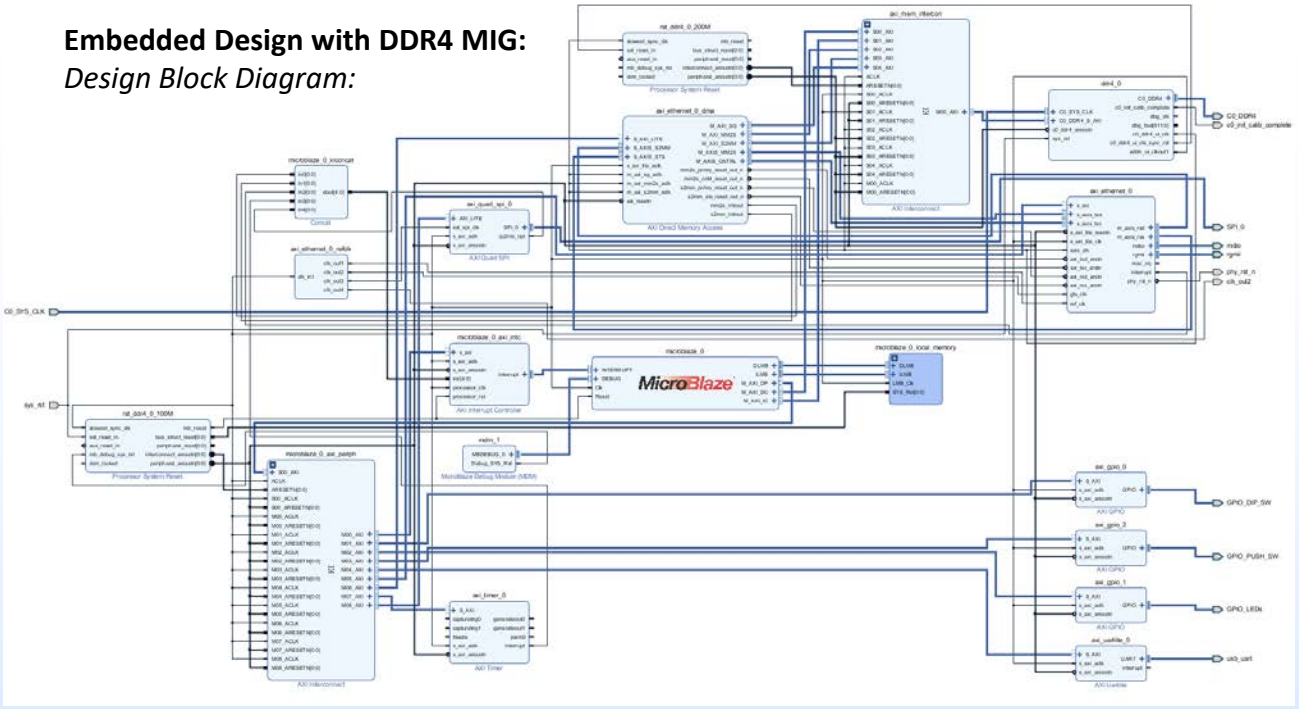


Timing:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.068 ns	Worst Hold Slack (WHS):	0.013 ns	Worst Pulse Width Slack (WPWS):	0.298 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	12365	Total Number of Endpoints:	12365	Total Number of Endpoints:	5603

Embedded Design with DDR4 MIG:

Design Block Diagram:



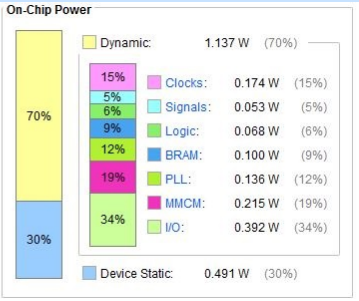
Utilization:

Resource	Utilization	Available	Utilization %
LUT	23059	242400	9.51
LUTRAM	1817	112800	1.61
FF	31251	484800	6.45
BRAM	48	600	8.00
IO	112	312	35.90
BUFG	14	480	2.92
MMCM	2	10	20.00
PLL	2	20	10.00

Power:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.628 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**28.0°C**
Thermal Margin:	57.0°C (29.9 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0.088 W
Confidence level:	Low



Timing:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.178 ns	Worst Hold Slack (WHS):	0.024 ns	Worst Pulse Width Slack (WPWS):	0.124 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	79982	Total Number of Endpoints:	79390	Total Number of Endpoints:	34208